WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate;

a gate region on top of the substrate;

a first and second sidewall liners situated on a first and second sides of the gate region respectively, the first and second sidewall liners having a vertical part contacting sidewalls of the gate region and a horizontal part contacting the substrate; and

a first and second recessed spacers situated on top of the first and second sidewall liners respectively,

wherein a height of the first and second recessed spacers is lower than a height of the sidewall liner, and

wherein the horizontal part of each sidewall liner is shorter than the corresponding recessed spacer on top thereof.

2. The device of claim 1 wherein the height of the recessed spacer is at least 50 Å lower than the height of the vertical part of the sidewall liner.

3. The device of claim 1 wherein the horizontal part of each gate sidewall liner is at least 10 Å shorter than the recessed spacers.

4. The device of claim 1 wherein the gate region further includes a gate dielectric and electrode layers.

5. The device of claim 4 wherein the height of the gate region does not exceed 1800Å.

6. The device of claim 1 wherein the recessed spacer is SiN based.

7. The device of claim 1 wherein the recessed spacer further includes Ge, Ar, or O_2 based impurities.

8. The device of claim 1 wherein the sidewall liner is oxide based.

9. The device of claim 1 further comprising a contact etching stopper (CES) layer formed over the recessed spacer with a predetermined stress level.

10. The device of claim 9 wherein the CES layer imposes a compressive stress.

11. The device of claim 9 wherein the CES layer imposes a tensile stress.

12. The device of claim 9 wherein the stress level of contact etching stopper layer is larger than 200M Pa.

13. The device of claim 9 wherein the thickness of the CES layer is smaller than 600Å.

14. A method for fabricating at least one semiconductor device having

a gate region and recessed spacers, comprising:

forming a substrate;

forming a gate region on top of the substrate, the gate region having a gate electrode and a gate dielectric region;

forming two sidewall liners confining the gate region therebetween;

forming two spacers on top of the sidewall liners on both sides of the gate region, a height of the spacers matching substantially a height of the sidewall spacers;

reducing the width of the sidewall liners underneath the spacers to pull back from an edge of each spacer by a predetermined distance; and

forming two recessed spacers by reducing the height of the formed spacers,

wherein the reduced spacer height reduces device channel stress.

15. The method of claim 14 wherein the forming two spacers further includes depositing spacer material and etching the deposited spacer material so that the top of the spacers slope down from the top of the sidewall liners to a horizontal part of the sidewall liner that extends along the substrate from the gate region.

16. The method of claim 14 wherein the reducing further includes:

forming an oxide layer over the spacers, the sidewall liners, and the gate region;

etching the oxide off within a predetermined time period so that the width of the sidewall liners are pulled back for a predetermined distance.

17. The method of claim 14 wherein forming two recessed spacers further includes selectively etching the spacers to reduce at least 50Å in the height of the spacers to form the recessed spacers.

18. The method of claim 14 further comprising introducing one or more impurities to the spacers to further reduce the device channel stress.

19. The method of claim 14 wherein the predetermined distance pulled back from the edge of each spacer is at least 10Å.

20. The method of claim 14 further comprising forming a contact etch stoper (CES) layer over the recessed spacers for further modifying the device channel stress.

21. The method of claim 20 wherein the CES layer imposes a compressive stress.

22. The method of claim 20 wherein the CES layer imposes a tensile stress.

23. A transistor comprising:

a substrate;

a gate electrode on top of the substrate;

a first and second "L" shaped gate sidewall liners confining the gate electrode therebetween, the first and second sidewall liners having a vertical part contacting sidewalls of the gate electrode and a horizontal part contacting the substrate; and

a first and second recessed spacers situated on top of the first and second sidewall liners respectively; and

a contact etching stopper (CES) layer situated over the recessed spacers,

wherein a height of the first and second spacers is lower than a height of the gate sidewall liners and a width of the gate sidewall liners is shorter than that of the first and second spacers, and

wherein the recessed spacers are doped with predetermined impurities for modifying a channel stress of the transistor.

24. The transistor of claim 23 wherein the recessed spacers are at least 50 Å lower than the gate sidewall liners.

25. The transistor of claim 23 wherein the gate sidewall liners are at least 10Å shorter than the recessed spacers.

26. The transistor of claim 23 wherein the impurities doped into the recessed spacers includes Ge, Ar, or O_2 based impurities.

27. The transistor of claim 23 wherein the CES layer formed over the recessed spacers is thicker than the recessed spacers.

28. The transistor of claim 23 wherein the contact etching stopper layer is thinner than 600Å.

29. The transistor of claim 23 wherein the contact etching stopper layer imposes a tensile stress less than 1.5G Pa.

30. The transistor of claim 23 wherein the contract etching stopper layer imposes a compressive stress less than 1.0G Pa.

31. A semiconductor device comprising:
a substrate;
a gate region on top of the substrate;
two sidewall liners situated on two sides of the gate region; and
a spacer situated on top of each sidewall liner,
a contact etching stopper layer over the spacers,
wherein the contact etching stopper layer is thicker than the spacer.

32. The device of claim 31 wherein the thickness of contact etching stopper layer is smaller than 600 Å.

33. The device of claim 31 wherein the contact etching stopper layer imposes tensile stress.

34. The device of claim 33 wherein a stress level of the contact etching stopper layer is less than 1.5G Pa.

35. The device of claim 31 wherein the contact etching stopper layer imposes compressive stress.

36. The device of claim 35 wherein a stress level of the contact etching stopper layer is less than 1.0G Pa.

37. A semiconductor device comprising:
a substrate;
a gate region on top of the substrate;
two "L" shaped sidewall liners situated on two sides of the gate region;
a recessed spacer situated on top of each sidewall liner; and
a contact etching stopper layer formed over the spacers, the sidewall, and the gate region,
wherein the contact etching stopper layer is thicker than the spacer, and
wherein the sidewall liner is higher and wider than the recessed spacer.

38. The device of claim 37 wherein the thickness of the contact etching stopper layer is smaller than 600 Å.

39. The device of claim 37 wherein the contact etching stopper layer imposes a tensile stress.

40. The device of claim 39 wherein a stress imposed by the contact etching stopper layer is less than 1.5G Pa.

41. The device of claim 37 wherein the contact etching stopper layer imposes a compressive stress.

42. The device of claim 41 wherein a stress imposed by the contact etching stopper layer is less than 1.0G Pa.